REMARKS/ARGUMENTS

The present Amendment is in response to the Office Action having a mailing date of March 27, 2002. Claims 1-20 are pending in the present Application. Claims 1-20 are rejected. Applicant has amended the claims 1, 3, 5, 8, 14-15, and 18 for clarification. Claims 2, 6-7, 9, 15, and 20, have been cancelled. Consequently, claims 1, 3-4, 8, 10-14, 16-19 remain pending in the present application.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration allowance and passage to issue of the present application are respectfully requested.

Double Patenting

The Examiner states:

> **2. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,348,812. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations are similar.**

Applicant will file a terminal disclaimer upon allowance of the application.

35 USC §102 Rejections

The Examiner states:

> **Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Kondou et al (4,876,466).**
>
> **Regarding clam 1, Kondou shows a dynamic (dynamic type, col. 6, lines 14-19) programmable logic array comprising:**
>
> **At least one logic plane (AND PLANE, Fig. 3A); and**

At least one reprogrammable evaluate module (200) within the at least one logic plane, the at least one reprogrammable evaluate module (Fig. 4B, 5A) including a first program input (B), a second program input (a or W), a storage element (Fig. 5A) coupled to the first and second program inputs, and input pass transistor (202, Fig. 4A; Figure 6 shows 202 transistor) coupled to the output of storage element and an evaluate transistor (100, Fig. 4B) coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

Regarding claim 2, Kondou shows the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to a control input (d) and a gate of the evaluate transistor (see Fig. 4A, 5A & 6).

Regarding claim 3, Kondou shows the storage element comprises a multiple transistor register.

Regarding claim 4, Kondou shows the multiple transistor register comprises:

A program data pass transistor, which includes a gate source and drain, the source (B), Fig. 5A) of the program data pass translator is coupled to the first program input and the gate is coupled to the second program input (W);

A first inverter (a top inverter, Fig. 5) whose input is coupled to the drain of the program data pass transistor and whose output is coupled to the output of the storage element;

and

A second inverter (a bottom inverter) whose input is coupled to the output of the first inverter and whose output is coupled to the input of the first inverter, wherein the storage element is written by placing a desired value on the first program input and asserting the second program input.

Regarding claim 8, Kondou shows a dynamic programmable logic array (Fig. 3A) comprising:

A first logic plane (AND PLANE);
A first reprogrammable evaluate module (200) with the first logic plane;
A second logic plane (OR PLANE) coupled to the first logic plane and for providing an output (O); and
A second reprogrammable evaluate module (200) within the second logic plane,
wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

The limitations of claims 9-17 are rejected as above claims.

3. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Hanrahan et al (6,311,200).

Regarding claim 1, Hanrahan shows a dynamic programmable logic array comprising:

At least one logic plane (24, Fig. 1); and
At least one reprogrammable evaluate module (76, Fig. 3) within the at least one logic plane, the at least one reprogrammable evaluate module including a first program input (DATA INPUT, Fig. 7), a second program input (WRITE SELECT), a storage element (NOR-gate and inverter) coupled to the first and second program inputs, and input pass transistor (82) coupled to the output of storage element and an evaluate transistor (84) coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

Regarding claim 2, Hanrahan shows the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and a gate of the evaluate transistor (see Fig. 3).

Regarding claim 3, Hanrahan shows the storage element comprises a multiple transistor register (transistors are inherent elements from NOR-gate and inverter).

Regarding claim 5, Hanrahan shows an evaluate disable transistor (86) which includes a gate, source and drain, the gate is coupled to the output of the storage element, the source is coupled to the gate of the evaluate transistor, and the drain is coupled to the ground; and the output of the storage element turns on one of the input pass transistor or the evaluate disable transistor at any given time.

The limitations of claims 14-15 and 18 are rejected as above claims.

For the above-mentioned reasons the independent claims are allowable over the cited references. Moreover dependent claims 3, 4, 10-13, and 16-19 are allowable since they depend from an allowable base claim.

Applicant respectfully requests reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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April 8, 2004
Date

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